WHAT IS CLAIMED IS:

1. A method of forming a semiconductor device, the method comprising:

providing a substrate with one or more shallow trench isolations (STI) formed thereon;

forming a protective layer on a first region of the substrate, the first region encompassing a portion of at least one STI;

forming one or more semiconductor structures in a second region, the second region not being covered by the protective layer; and

removing the protective layer;

wherein the portion of the STI located in the second region is partially removed with respect to the STI located in the first region.

2. The method of claim 1 wherein the semiconductor device is a memory cell.

3. The method of claim 1 wherein the semiconductor device includes a floating gate transistor.

4. The method of claim 1 wherein the protective layer is an oxide.

5. A method of forming a semiconductor device, the method comprising:

providing a substrate with one or more shallow trench isolations (STI) filled with a dielectric material formed therein, the substrate having an oxide layer and a first poly layer formed thereon;

forming a protective layer on the first poly layer in a first region of the substrate;

fabricating in a second region one or more semiconductor structures, the semiconductor structures utilizing at least one of the first poly layer and the oxide layer in a second region, the second region not being covered by the protective layer;

forming on the substrate a second poly layer; and

removing the first poly layer, the protective layer, and the second poly layer from the first region.

6. The method of claim 5 wherein the dielectric material adjacent to the first region is a different height than the dielectric material adjacent to the second region.

7. The method of claim 5 wherein the semiconductor structures include a memory cell.

1 8. The method of claim 5 wherein the semiconductor structures include a floating
2 gate transistor.

1 9. The method of claim 5 wherein the protective layer is an oxide.

1 10. The method of claim 5 further comprising the step of doping the first poly layer in
2 the second region.

1 11. The method of claim 5 wherein the step of removing the second poly layer is
2 performed by an anisotropic etching step.

1 12. The method of claim 5 wherein the step of removing the oxide layer is performed
2 by an anisotropic etch process.

1 13. The method of claim 5 wherein the first region is a periphery region of a memory
2 device and the second region is a cell region of the memory device.

14. A method of forming a semiconductor device, the method comprising:

providing a substrate with one or more shallow trench isolations (STI) filled with an STI filler formed therein, the substrate having an oxide layer formed on the substrate and a first poly layer formed on the oxide layer;

forming a protective layer on the first poly layer and the STI filler in a first region of the substrate;

implanting exposed portions of the first poly layer;

fabricating in a second region one or more semiconductor structures such that the STI filler located in the second region is partially removed; and

removing the protective oxide, and the first poly layer.

15. The method of claim 14 wherein the semiconductor device is a memory array.

16. The method of claim 14 wherein the semiconductor device includes a floating gate transistor.

17. The method of claim 16 wherein the device layers include an inter-poly oxide layer and a gate poly layer.

18. The method of claim 14 wherein the protective layer is an oxide.

19. The method of claim 14 wherein the first region is a periphery region of a memory device and the second region is a cell region of the memory device.

20. The method of claim 14 wherein the step of removing the second poly layer is performed by an anisotropic etching step.

21. The method of claim 14 wherein the step of removing the oxide layer is performed by an anisotropic etch process.

22. The method of claim 14 wherein the step of removing the protective layer is performed by an anisotropic etch process.

23. The method of claim 14 wherein the step of removing first poly layer is performed by an isotropic etch process.